A Five-Decade Dynamic-Range Ambient-Light-Independent Calibrated Signed-Spatial-Contrast AER Retina With 0.1-ms Latency and Optional Time-to-First-Spike Mode

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***Abstract*—Address Event Representation (AER) is an emergent technology for assembling modular multiblock bio-inspired sensory and processing systems. Visual sensors (retinae) are among the first AER modules to be reported since the introduction of the technology. Spatial-contrast AER retinae are of special interest since they provide highly compressed data flow without reducing the relevant information required for performing recognition. The reported AER contrast retinae perform a contrast computation based on the ratio between a pixel's local light intensity and a spatially weighted average of its neighborhood. This resulted in compact circuits but with the penalty of all pixels generating output signals even if they sensed no contrast. In this paper, we present a spatial-contrast retina with a signed output: Contrast is computed as the relative difference (not the ratio) between a pixel's local light and its surrounding spatial average and normalized with respect to ambient light. As a result, contrast is ambient light independent, includes a sign, and the output will be zero if there is no contrast. Furthermore, an adjustable thresholding mechanism has been included, such that pixels remain silent until they sense an absolute contrast above the adjustable threshold. The pixel contrast-computation circuit is based on Boahen's biharmonic operator contrast circuit, which has been improved to include mismatch calibration and adaptive-current-based biasing. As a result, the contrast-computation circuit shows much less mismatch, is almost insensitive to ambient light illumination, and biasing is much less critical than in the original voltage biasing scheme. The retina includes an optional global reset mechanism for operation in ambient-light-independent Time-to-First-Spike contrast-computation mode. A 32 × 32 pixel test prototype has been fabricated in 0.35-μm CMOS. Experimental results are provided.**

***Index Terms*—Address-event-representation, analog circuits, artificial retina, bio-inspired circuits, calibration, contrast sensors, image sensors, low power circuits, spiking circuits, transistor mismatch.**

I. Introduction

ADDRESS event representation (AER) is a spike-based signal representation hardware technique for communicating spikes between layers of neurons in different chips. AER was first proposed in 1991 in one of the Caltech research laboratories [1], [2] and has been used since then by a wide community of neuromorphic hardware engineers. A variety of AER visual sensors can be found in the literature, such as simple luminance to frequency transformation sensors [3], Time-to-First-Spike (TFS) coding sensors [4]–[7], foveated sensors [8], [9], more elaborate transient detectors [10], [11], motion sensing and computation systems [12]–[16], and spatial and temporal filtering sensors that adapt to illumination and spatiotemporal contrast [17], [18].

Spike-based visual sensors can code their output signals using rate or TFS coding. When using rate coding, each pixel is autonomous and continuously generates spikes at a frequency that is proportional to the signal to transmit (such as luminance or contrast). Under such circumstances, there are no video frames, so that sensing and processing are continuous and frame-free. When using TFS coding, a global system-wide reset is provided, and each pixel encodes its signal by the time between this reset and the time of the only spike it generates. Sensing and processing are frame constraint. However, TFS is a highly compressed coding scheme (each pixel generates at the most one spike per frame), and frame time can be dynamically adjusted to an optimum minimum by subsequent processing stages. TFS coding and related concepts were originally proposed by Thorpe based on neurophysiological and psycophysical experiments [19], and they have evolved to very high speed image-processing software tools [20].

Spatial-contrast AER retina sensors are of special interest. Computing contrast on the focal plane significantly reduces data flow, while relevant information for shape and object recognition is preserved. In a conventional luminance sensor (a commercial camera), all pixels are sampled with a fixed period, and its light intensity (integrated over this period) is communicated out of the sensor to the next stage. In an AER sensor, pixels are not sampled. On the contrary, the pixels are the ones who initiate an asynchronous communication cycle, called "event," when a given condition is satisfied. For example, a spatial-contrast retina pixel would send an event whenever the computed local contrast exceeds a given threshold.

Previously reported plain spatial-contrast retinae [21], [22] compute a contrast current per pixel $I_{\rm cont}(x,y)$ as the ratio between a pixel's locally sensed light intensity $I_{ph}(x,y)$ and a spatially weighted average of its surrounding neighborhood $I_{\rm avg}(x,y)$ computed with some kind of diffusive network

$$I_{\rm cont}(x,y) = I_{\rm ref}\frac{I_{ph}(x,y)}{I_{\rm avg}(x,y)} \tag{1}$$

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TABLE I
COMPARISON BETWEEN SOME AER RETINA SENSOR DEVICES

	Cul03 [3]	Chen07 [6]	Licht08 [11]	Zagh04 [17]-[18]	Ruedi03 [4]	Costas07 [22]	This work
Functionality	Luminance to Frequency	Luminance to TFS	Temporal Contrast to Number of Events	Spatial and Temporal Contrast to Frequency	Spatial Contrast Magnitude and Direction to TFS	Spatial Contrast to Frequency	Spatial Contrast to Frequency or TFS
Light to Time Restriction	YES	YES	NO	NO	YES	NO	NO
Latency	120μs - 125s	10μs - 1s	15μs - 400μs (strong biases); 0.9ms - 4ms (nominal biases)	not reported	2ms - 150ms	not reported	0.1ms - 10ms
Dynamic Range	120dB	>100dB	120dB	50dB	110dB	100dB	100dB
Spatial Contrast computation	N/A	N/A	N/A	diffusive grid neighbourhood	4 nearest pixels (up, right, left, bottom)	diffusive grid neighbourhood (adjustable up to 10 pixels)	diffusive grid neighbourhood (adjustable up to 10 pixels)
FPN	4%	4.6%	2.5%	1-2dec	1.7%	6.6%	0.90%
Power	3-71mW	N/A	24mW	63mW	300mW	33μW - 10mW	0.66 - 6.6mW

where I_{ref} is a global scaling current. Since this is always positive, let us call it "unipolar" contrast computation, with contrast being computed as the ratio between two photocurrents. This yielded circuits where no subtraction operation was required. This was crucial to maintain mismatch (and precision) at reasonable levels. Note that, for computing I_{avg} and I_{cont}, circuits have to handle directly photocurrents, which can be as low as pico amperes or less. Performing a simple mirroring operation introduces mismatches with errors on the order of 100% [23]. This can be overcome by increasing transistor area, but then, leakage currents may become comparable to the available photocurrents. Consequently, while handling photocurrents, it is desirable to keep complexity at a minimum. Therefore, from a circuit point of view, the way of computing contrast, as in (1), was very convenient. However, this presents an important drawback: When there is no contrast ($I_{\text{avg}} = I_{ph}$), then $I_{\text{cont}} \neq 0$. In an AER circuit, this means that a pixel sensing no contrast will be sending out information (events) and consuming communication bandwidth on the AER channels. This is contrary to the advantages of AER (where it is expected that only information-relevant events will be transmitted) and contrary to the advantages of computing contrast at the focal plane (so that only contrast-relevant pixels need to send information). In a prior work [22], although spatial contrast was computed by (1) in the retina, postprocessing with AER (convolution) modules was added to effectively compute the Weber Contrast[1] as the signed quantity

$$I_{\text{cont}}(x,y) = I_{\text{ref}} \left(\frac{I_{ph}(x,y)}{I_{\text{avg}}(x,y)} - 1 \right). \tag{2}$$

[1]Weber Contrast is defined as $WC = (I - I_{\text{avg}})/I_{\text{avg}}$ for a pixel photocurrent with respect to its neighborhood average photocurrent or as $WC = (I_1 - I_2)/(I_1 + I_2)$ between two adjacent pixels or regions. Both expressions are equivalent by making $I = I_1$ and $I_{\text{avg}} = (I_1 + I_2)/2$.

This reduced significantly the data flow (from about 400 keps to about 10 keps),[2] but also at the expense of reducing pixel speed response and contrast sensitivity by a factor of about ten.

In this paper, we present a new spatial-contrast retina design [25], where the contrast computation follows (2). The design is based on the original contrast-computation circuit by Boahen and Andreou [21], which has been improved to overcome its inherent limitations on mismatch, ambient light dependence, and critical controllability. Section II discusses related work and summarizes a prior AER mismatch-calibrated contrast retina pixel [22] that followed (1), Section III summarizes briefly Boahen's spatial-contrast-computation circuit, Section IV summarizes a more compact calibration circuit than the one used in [22] and which has been used in the present design, and Section V introduces the new pixel design. Finally, Section VI provides experimental characterization and test results.

II. PREVIOUS DESIGNS

A variety of AER retina sensors have been reported, from which we have selected a few for comparison purposes. Table I summarizes and compares their functionalities and performance figures. Three types of functionalities are considered: sensing pixel luminance, sensing pixel temporal contrast, and sensing pixel spatial contrast with respect to a given neighborhood. For (spike) signal coding, three methods are used: signal to frequency (rate) coding, signal to number of events (NE) coding, and signal to TFS coding. When using rate coding (as in [3], [17], [18], and [22]), a current that carries the information of interest (luminance; contrast) is fed to an integrate-and-fire circuit whose spike frequency is controlled by the current. For NE coding (as in [11]), every time the light, sensed by a pixel,

[2]Keps stands for "kiloevents per second."

changes by a relative amount, a new spike is generated. In TFS coding (as in [4] and [6]), the information signal is also fed to an integrate-and-fire circuit, but the integrators are periodically and globally reset and only fire one spike between consecutive resets. This way, the information is coded as the time between the global reset and the pixel spike time. For a luminance retina [3], [6], the photocurrent is the one to be integrated. Since light (photocurrent) can change over many decades, this results in timings that are directly dependent on ambient light. Consequently, the dynamic range of light-sensing capability is directly transformed into the latency variation of the output. This is a severe practical restriction, labeled in Table I as the "Light to Time Restriction." For contrast computations (either spatial or temporal), light difference is normalized to average light, so that contrast is (by definition) independent of ambient light. Consequently, these retinae should not suffer from the "Light to Time Restriction." This is the case for all contrast retinae in Table I, except for [4]. The reason is that, in [4], for each frame, there are two separate steps in time. The first one uses a Light to Time integration (which lasts between 0.5 μs and 150 ms, depending on ambient light) to obtain a voltage representation of pixel contrast. The second step transforms these voltages into a TFS representation requiring an ambient-light-independent time of about 2 ms. In this paper, we present a spatial-contrast retina whose ambient-light-independent pixel spatial contrast can be either coded as frequency or TFS.

In a previous spatial-contrast AER retina design [22], each pixel computes local spatial contrast as a ratio

$$I_{\rm cont}(x,y) = I_{\rm ref}(x,y)\frac{I_{\rm avg}(x,y)}{I_{\rm ph}(x,y)} \tag{3}$$

where $I_{\rm ph}(x,y)$ is the pixel photocurrent, and $I_{\rm avg}(x,y)$ is a neighborhood pixel photocurrent average computed by a diffusive grid [26]. The resulting current $I_{\rm cont}(x,y)$ is thus proportional to a unipolar contrast [as in (1)] and is fed to an integrate-and-fire neuron generating spikes with a frequency proportional to $I_{\rm cont}(x,y)$. Scaling current $I_{\rm ref}(x,y)$ is made locally trimmable for each pixel in order to compensate for mismatch. As a result, interpixel contrast computation mismatch could be reduced from about $\sigma \approx 60\%$ to $\sigma \approx 6\%$ using 5-bit pixel registers to control $I_{\rm ref}(x,y)$. Pixel complexity was kept relatively simple (104 transistors + 1 capacitor), owing to the unipolar nature of the contrast computation, and the whole pixel could be fit into an area of 58 μm $\times$ 56 μm in a 0.35-μm CMOS process. The main drawback is that pixels with no contrast would generate output events at a constant rate proportional to $I_{\rm ref}$. To overcome this, a 4-AER-module system was assembled [22] to subtract this offset and compute effectively a signed contrast as in (2). However, contrast sensitivity was reduced by a factor of eight, thus reducing its speed response, as well as contrast sensitivity.

III. Boahen Spatial-Contrast Pixel

In the design presented in this paper, the speed and contrast sensitivity reduction problem is solved by performing all the signed-spatial-contrast computation at the sensor chip using an improved version of Boahen's original biharmonic contrast-computation circuit [21]. The continuous approximation

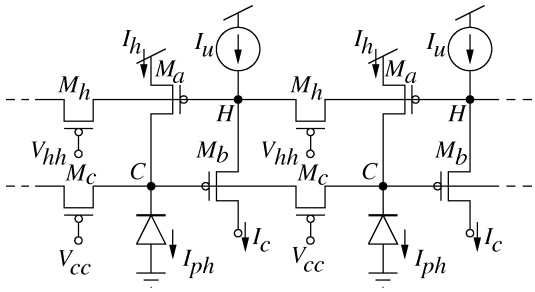

Fig. 1. Boahen original contrast-computation circuit.

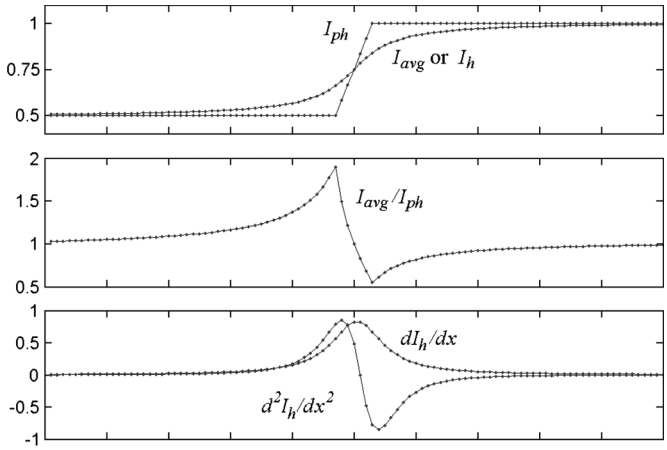

Fig. 2. Interpretation of spatial-contrast computations.

of Boahen's pixel circuit, shown in Fig. 1, solves approximately the following [26]:

$$I_h(x,y) = I_{ph}(x,y) + a\nabla^2 I_c(x,y) \tag{4}$$

$$I_c(x,y) = I_u - b\nabla^2 I_h(x,y). \tag{5}$$

Solving for I_h results in the biharmonic equation used in computer vision to find an optimally smooth interpolating function of the stimulus I_{ph}[27]. Consequently, the output $I_c(x,y)$ is a second-order spatial derivative of the interpolation I_h according to (5). Since the interpolation is a spatially integrated version of the stimulus, I_c can be interpreted as a version of a first-order derivative of the stimulus, therefore, spatial contrast. This can also be understood with the help of Fig. 2. The top trace shows a step stimulus I_{ph} and its spatial average ($I_{\rm avg}$ or I_h). The center trace shows the contrast computation as $I_{\rm avg}/I_{ph}$ (as was done in [22]), and the bottom trace shows the contrast computation as the second-order spatial derivative of I_h. Both are equivalent, although not identical. According to (5), I_c includes a dc term I_u.

The original circuit implementation of this model suffered from a series of drawbacks. First, mismatch was comparable to output signal. Second, output signal would degrade for the same contrast stimulus when changing lighting conditions. Third, contrast gain had to be adjusted through critically sensitive bias voltages with very narrow tuning range. All three drawbacks have been improved with the present implementation.

IV. Compact Calibration Circuit

We reduce mismatch by introducing calibration. One dominant source of mismatch is the dc component I_u in (5). Since this current is set constant, independent of lighting conditions,

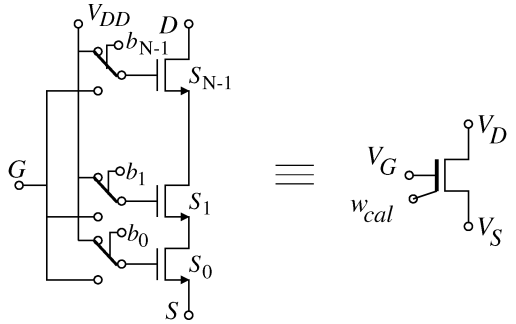

Fig. 3. Digitally controlled length MOS used for calibration.

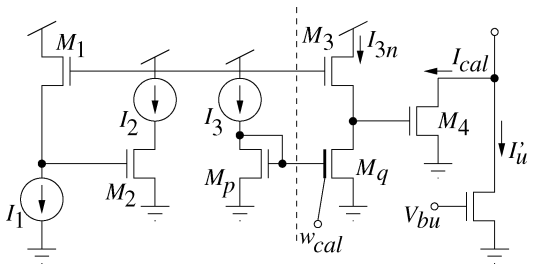

Fig. 4. Translinear tuning circuit.

we can directly subtract it with a trimmable current source. The output current will thus be directly the signed contrast current we were looking for. To implement the trimmable current source, we follow the recently reported very compact circuit based on series transistors association [29]. Fig. 3 shows the basic principle behind this circuit. Each switched MOS operates as a segment of an effective longer MOS whose length is controlled digitally by switching individual segments from ohmic to saturation, and vice versa. The key consists of making each segment to contribute approximately as a power of two to the total length. The digital control word $w_{\rm cal} = \{b_{N-1}, \ldots, b_1 b_0\}$ sets the state of the switches. As a result, the effective length is digitally controlled as in a digital-to-analog conversion. On the right of Fig. 3, we show the symbol of a digi-MOS (digitally controlled MOS), which we use to represent the circuit on the left.

Fig. 4 shows the circuitry used to subtract the dc component I_u of the contrast current. Transistors to the left of the dashed line are shared by all pixels and are located at the chip periphery, while those to the right are replicated for each pixel. Current I'_u sets the subtracting dc level (while also introducing mismatch), while $\{I_1, I_2, I_3\}$ are adjusted so that $I_{\rm cal}$ has a tuning range covering the interpixel mismatch. Transistors M_{1-4} form a translinear loop [26], thus $I_{\rm cal} = I_1 I_2 / I_{3n}$. Moreover, I_{3n} is a mirrored version of I_3 by transistors M_p and M_q. Transistor M_q is the digi-MOS of Fig. 3. Consequently, $I_{\rm cal}$ is proportional to the pixel calibration word $w_{\rm cal}(x, y)$, which is stored in in-pixel static RAM latches loaded at start-up. Note that current $I_{\rm cal}$ could have been generated directly by current mirror $M_p - M_q$. However, in this case, if one wants to scale $\{I_u, I_{\rm cal}, I'_u\}$ globally (to adjust the retina output frequency range), the circuit would change the current through the calibration branch containing M_q. On the contrary, with the circuit in Fig. 4, one can scale $\{I_u, I_{\rm cal}, I'_u\}$while keeping the calibration branch current I_{3n} (and I_3) constant, and scale through peripheral currents I_1 and/or I_2. This way, calibration degrades less when tuning the output frequency range.

In the section on experimental results, we explain how we proceed to perform calibration.

V. Improved Signed-Spatial-Contrast Pixel

Fig. 5 shows the schematics of all pixel circuitry. Fig. 5(a) shows an overall block diagram, indicating the signals interchanged between blocks. The pixel contains three main parts: 1) the photo-sensing and contrast-computation part, including calibration, which provides the ambient-light-independent contrast current $I_{\rm cont}$; 2) the integrate-and-fire part, which includes refractory circuitry, thresholding, and TFS mode; and 3) the pixel AER communication circuitry that sends out events to the periphery. Let us now describe each one.

A. Photo Sensing and Contrast Computation

Fig. 5(b) shows how Boahen's contrast-computation circuit has been modified to include a current-biasing scheme for controlling the original voltages V_{cc} and V_{hh} in Fig 1. This way, gate voltages V_{cc} and V_{hh} tend to follow voltage excursions at nodes "C" and "H."

The first advantage of this is that biasing will adapt to ambient light conditions. For example, if all photodiode currents are scaled up/down by the same factor, the voltage at all nodes "H" will follow it logarithmically. Since I_u is constant, the voltage at node "C" will thus also follow the same shift. Since bias currents I_{hh} and I_{cc} are kept constant, the gate voltages of transistors M_h and M_c will thus follow also this same global voltage shift, adapting themselves to the global light change.

The second advantage of this current-biasing scheme is that it attenuates mismatch. After doing careful mismatch analysis and identifying the main sources of mismatch for this circuit, one can find out that transistor M_a and current I_u are the dominant sources of mismatch. This can be understood as follows. Mismatch in I_u goes directly into the dc offset of I_c, which will be calibrated by $I_{\rm cal}$. Mismatch of M_b is less critical because its interpixel gate voltage (node "C") variability affects the bottom diffusive grid and the computation of the average current I_h. Thus, its variability impact is attenuated by the average computation. However, M_a mismatch (V_{gs} variation of M_a) changes directly the source voltage of M_b, affecting directly the gain of contrast output [coefficient "b" in (5)], whose effect is not directly calibrated by $I_{\rm cal}$. Consequently, M_a needs to be sized to minimize mismatch. The effect of I_u will be compensated by calibration, and the effect of M_a will be attenuated by the current-biasing scheme. Note that mismatch in all M_a transistors will introduce random voltage variations at nodes "H" and "C." These variations will be transformed into random lateral currents through transistors M_h and M_c. The random currents through M_h will be collected by output current I_c and can be compensated by calibration. However, random currents through M_c transistors operate as if they were generated by the photodiodes. Owing to the current-biasing scheme, an increase in "C" will increase the gate voltage of the new bottom NMOS transistor, increasing its source voltage, thus increasing the gate voltage of M_c, which will reduce the lateral random current. A similar effect will be happening for transistors M_h.

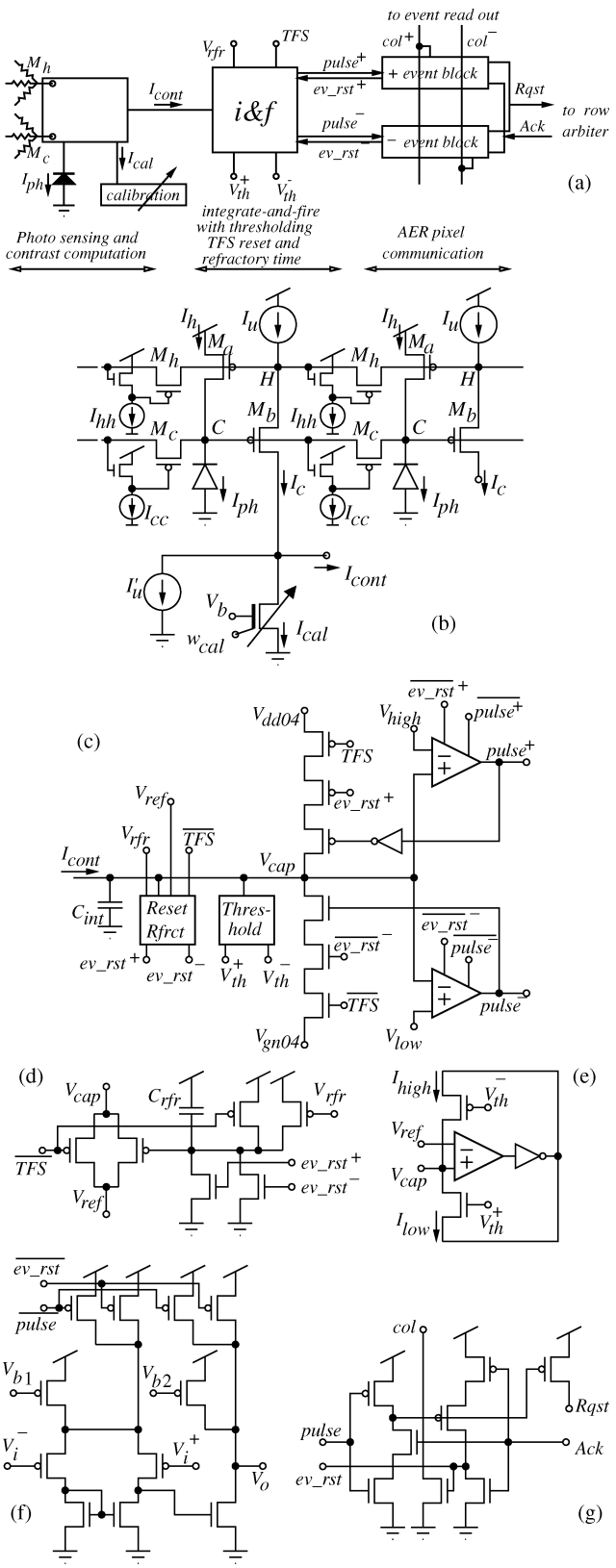

Fig. 5. Pixel schematics diagram. (a) Compact block diagram. (b) Detail of photo-sensing and contrast-computation circuits. (c) Detail of signed integrate-and-fire circuit. (d) Detail of reset and refractory circuits. (e) Detail of thresholding circuit. (f) Detail of comparators. (g) Detail of block circuit.

Finally, the third advantage is a more robust means for biasing the lateral transistors. In the original scheme, voltages V_{cc} and

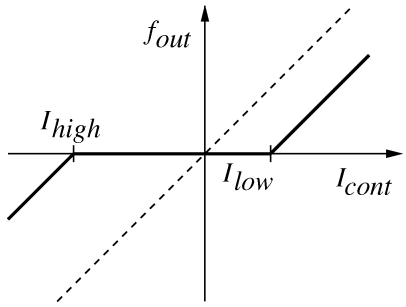

Fig. 6. Effect of contrast thresholding on the relationship between pixel output frequency and contrast current.

V_{hh} suffered from a very narrow and critical tuning range (about 100 mV or less). Now, bias currents I_{cc} and I_{hh} can be tuned over several decades while still perceiving their effect.

B. Integrate and Fire

Fig. 5(c) shows the integrate-and-fire block. Input contrast current $I_{\rm cont}$ is integrated on capacitor $C_{\rm int}$. Two comparators detect whether the capacitor voltage $V_{\rm cap}$ reaches an upper $(V_{\rm high})$ or lower (V_{low}) threshold, triggering the generation of a positive $(pulse+)$ or negative $(pulse-)$ event, respectively. To accelerate the comparisons, both comparators activate a positive feedback loop (from $V_{\rm cap}$ to V_{dd04} for a positive event or from $V_{\rm cap}$ to V_{gn04} for a negative event).

After the event generation, capacitor $C_{\rm int}$ is reset to the central voltage $V_{\rm ref}$. This is done by the reset circuit shown in Fig. 5(d). This reset mechanism includes a refractory timing circuit that inhibits the pixel from generating subsequent events before a refractory capacitor C_{rfr} has been discharged by the dc current source MOS controlled by V_{rfr}. The reset circuit also includes the global TFS mode reset signal, which resets all pixel capacitors $C_{\rm int}$ simultaneously. Note that this signal inhibits the positive feedback loops in Fig. 5(c). This allows resetting quickly those pixels generating an event when TFS becomes active.

Fig. 5(e) shows the minimum contrast thresholding circuit. A comparator detects whether the capacitor voltage is above or below $V_{\rm ref}$ and turns on either a positive $(I_{\rm low})$ or negative $(I_{\rm high})$ threshold current, which $I_{\rm cont}$ needs to exceed for producing an event. Fig. 6 shows the resulting relationship between integrate-and-fire circuit output frequency $f_{\rm out}$ and the input signed contrast current $I_{\rm cont}$ while bias voltages $V_{\rm th}^+$ and $V_{\rm th}^-$ are set to generate threshold currents $I_{\rm high}$ and $I_{\rm low}$, respectively. Naturally, threshold transistors would also introduce mismatch. Consequently, they were layed out with a large area of 2/20 μm.

Fig. 5(f) shows the two-stage comparators used in Fig. 5(c). At standby, they are biased at low current through V_{b1} and V_{b2}. However, during event generation, its bias current is increased. This increase starts when signals *pulse* start to depart from its resting voltage and stops after the pixel event reset signal *ev_rst* returns to its resting level. The comparator within the thresholding circuit in Fig. 5(e) does not have this feature, since this comparator only needs to detect whether the so far accumulated contrast for the pixel is positive or negative, which is a slow process compared to the event generation timings.

TABLE II
RETINA SPECIFICATIONS SUMMARY

technology	CMOS 0.35μm 4M 2P
power supply	3.3V
chip size	3.7 x 3.5 mm^2
array size	32 x 32
pixel size	81.5 x 76.5 μm^2
fill factor	2.0%
pixel complexity	131 transistors + 2 caps
current consumption	65μA @ 10keps
dynamic range	1-100k lux
post-calibration FPN	0.90% over 5 decades if ambient light
contrast sensitivity	4400 Hz/WC
temporal latency	0.1ms @ 50k-lux
maximum out event rate	22 Meps

C. AER Communication

Finally, the AER pixel communication part in Fig. 5(a) contains two identical "event block" circuits, which are shown in Fig. 5(g). These are standard AER pixel communication circuits taken from Boahen's row parallel event read-out technique [30]. When generating signed events, each pixel needs to provide two column event signals $col+$ and $col-$. This concept was already implemented and tested in prior designs [31] that required signed events.

VI. EXPERIMENTAL RESULTS

A 32×32 pixel test prototype AER signed-spatial-contrast retina chip has been designed and fabricated in a double poly four-metal 0.35-μm CMOS process with a power supply of $V_{DD} = 3.3$ V. Table II summarizes the chip specifications. Fig. 7 shows a microphotograph of the die, of size 3.7×3.5 mm^2. The whole chip, except the pad ring, is covered with the top metal layer, leaving openings for the photodiode sensors. Fig. 7 also shows the layout of a single pixel highlighting its components. Each pixel layout is a symmetrical speculation of its neighboring pixels. This way, noisy digital lines are shared among neighbors, as well as power supplies, and noise-sensitive bias lines. At the same time, noise-sensitive lines are separated from noisy ones. The pixel area is 81.5×76.5 μm^2, including routing.

A. Pixel Frequency Range

One of the corner pixels had its integrating capacitor node connected to a low-input-capacitance analog buffer for monitoring purposes. Pixel-integrating capacitors have a capacitance of about $C_{\text{int}} \approx 118$ fF (obtained from the layout extractor), while the corner pixel with monitoring buffer has a total capacitance of about $C_{\text{mntr}} \approx 196$ fF (estimated from layout extraction and simulation). Fig. 8 shows the recorded waveforms (for positive and negative currents) for this capacitor when turning off horizontal interactions among neighboring pixels [by turning off transistors M_h and M_c in Fig. 5(b)], and for a typical value of $I_u \approx 100$ pA. By changing I_u (with $I'_u = I_{\text{cal}} = 0$) or I'_u (while $I_u = I_{\text{cal}} = 0$), pixel oscillation frequency could be tuned between 1.2 Hz and 5 kHz. For the maximum frequency, the arbitrating periphery inserts varying delays. This is because all pixels are also firing with maximum frequency (even higher than the pixel we are observing, which has slightly higher integrating capacitance) and are collapsing the arbiter. Consequently, in a practical situation where only a small percentage of the pixels would fire with maximum frequency, they would be able to fire with a higher than 5 kHz max frequency.

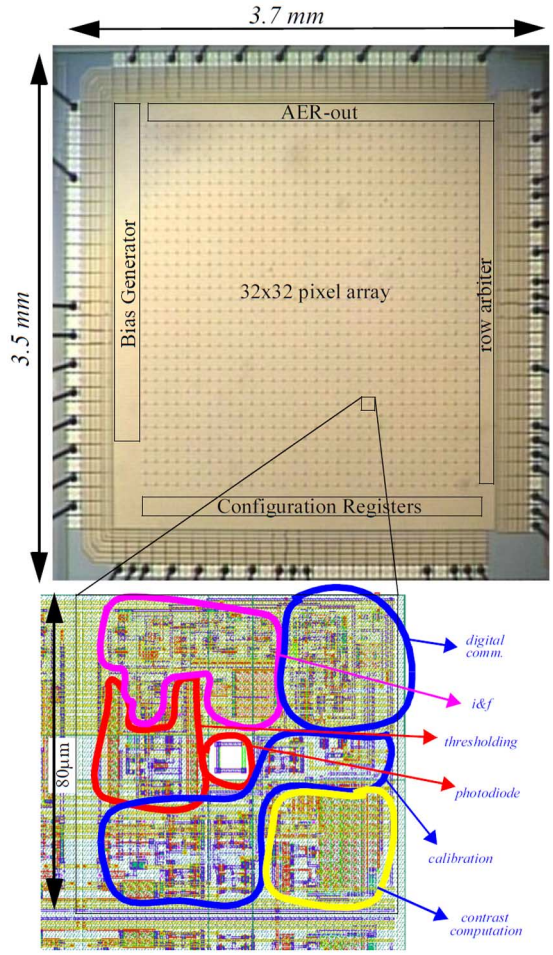

Fig. 7. Microphotograph of 2.5 mm × 2.6 mm die, and zoom-out view of 80 μm × 80 μm pixel (layout), indicating the location of its components.

B. Calibration

In order to use the retina properly, the first requirement is to calibrate it. For this, the retina was exposed to a uniform stimulus while biased for the following operation conditions: $I_u = 150$ pA, $V_{\text{ref}} = 1.65$ V, $V_{\text{high}} = 2.8$ V, $V_{\text{low}} = 0.45$ V, $I_{hh} = 10$ pA, and $I_{cc} = 5$ pA. Moreover, before calibration, we set $2I_{\text{cal}} = I'_u = 0$. Under these conditions, retina output events are recorded, from which one can obtain the firing frequency of each pixel. Next, we set current $I'_u = 80$ pA, so that the pixel with minimum frequency has a frequency close to zero (or slightly negative). Under these conditions, the resulting histogram of pixel frequency distribution is shown in Fig. 9(a). After this, the calibration circuit biases (I_1, I_2, and I_3 in Fig. 4) were set for optimum coverage of this distribution, and for each pixel, the optimum calibration word $w_{\text{cal}}(x, y)$ was found. This is computed offline by optimally combining biases $\{I_1, I_2, I_3\}$ and calibration words $w_{\text{cal}}(x, y)$. We allowed for a few outliers in order to minimize the residual standard deviation. One could also target to minimize the spread among the most

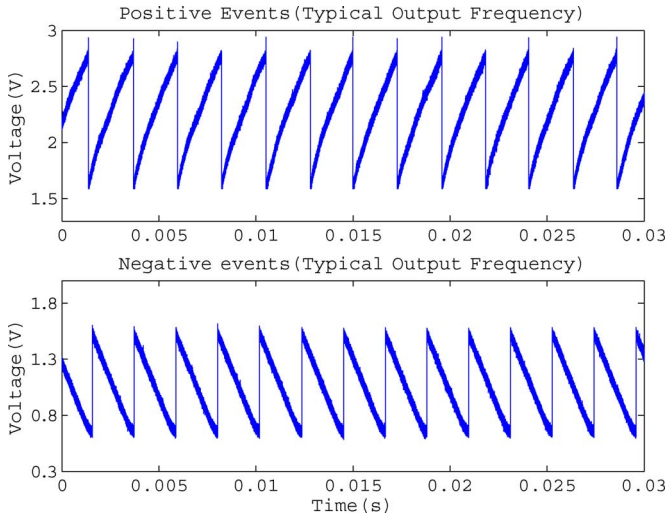

Fig. 8. Recorded waveforms at the integrating capacitor, under typical operating biases. The oscillation frequency is 466 Hz.

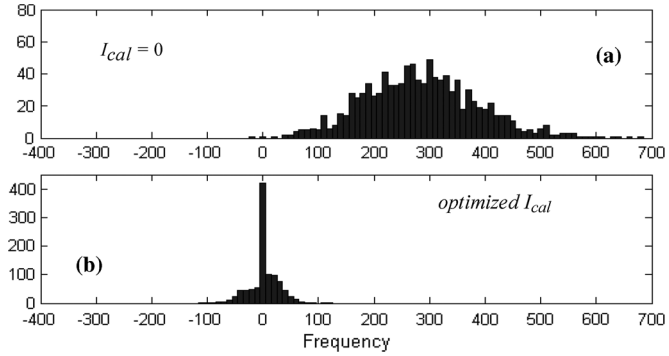

Fig. 9. Histograms of retina pixel frequency distribution (a) before and (b) after calibration.

extreme pixels at the expense of a higher standard deviation. After this process, the histogram of resulting calibrated pixel frequencies is shown in Fig. 9(b). The residual interpixel standard deviation is 26 Hz. As we will see later (in Section VI-D), the maximum contrast frequency for these biases is ± 4400 Hz. Consequently, postcalibration residual mismatch is $\sigma = 0.30\%$. Fig. 10 shows how the standard deviation of the postcalibration residual mismatch changes with illumination level. The figures show five superimposed graphs. Each one corresponds to performing calibration at different illumination levels (50, 15, 5, 1, and 0.25 klux).The worst case situation corresponds to calibrating at about 1 klux and using the retina at very high light conditions, resulting in a standard deviation of almost 140 Hz ($\sigma = 1.5\%$). On the other hand, the optimum situation corresponds to calibrating at 15 klux, which results to a standard deviation of less than 80 Hz ($\sigma = 0.9\%$) over the entire five decade range.

The calibration process is all done offline. However, it is conceivable to implement it fully on chip (through, for example, a vhdl-described state machine), since it only requires to expose the chip to uniform illumination (one can simply remove the optics), compare the pixel frequencies (for which not even a precise clock reference is required), and compute an optimum set of calibration weights.

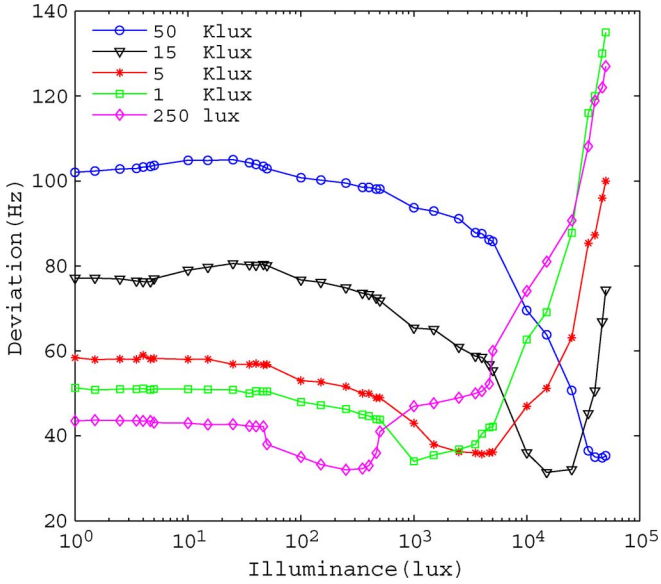

Fig. 10. Effect of ambient illumination on postcalibration residual mismatch standard deviation. Five curves are shown, each for calibrating at the given illumination level.

C. Contrast Step Response

Fig. 11 shows the retina response to a luminance step of different contrast levels, while thresholding is turned off. Input stimulus is printed paper, providing a static image with a half dark and a half gray side. The half-gray-side intensity is adjusted between 100% (white) and 30% (darkest gray). Table III indicates the relationship of the luminance steps, with the ratio of photocurrents between the gray and black parts, and the resulting Weber Contrast (defined as $(I_{\text{light}} - I_{\text{dark}})/(I_{\text{light}} + I_{\text{dark}})$). The left column in Fig. 11 shows this input stimulus image. The center column in Fig. 11 shows the retina output response before calibration, while the right column shows the retina response after calibration. The central gray level is zero pixel frequency. Brighter pixels are firing positively signed events, while darker pixels are firing negatively signed events. Absolute maximum pixel frequency was 250 Hz. Biasing conditions in Fig. 11 were $I_u = 150$ pA, $I'_u = 150$ pA, $V_{\text{high}} = 2.9$ V, $V_{\text{low}} = 0.4$ V, and $V_{\text{ref}} = 1.65$ V.

D. Contrast Sensitivity

An important characterization for a spatial-contrast retina is its contrast sensitivity: What is the output event rate for a given input contrast stimulus. We have characterized spatial-contrast sensitivity for the positive and negative event branches [see Fig. 5(a)] separately, since they have separate circuitry. Usually, under normal operation, the retina will be biased to have the same sensitivities for positive and negative events. However, there might be situations where one would prefer to set different contrast sensitivities for positive and negative events, and this retina offers this possibility. To characterize pixel contrast sensitivity, a gray level step stimulus (as shown in Fig. 11) of different contrast values was used. Pixel frequencies of the two columns with the highest activity (the ones just on the left and right of the stimulus center) were recorded. This process was repeated for different bias values for V_{high} and V_{low}, with $V_{\text{ref}} = 1.65$ V. The results are shown in Fig. 12(a). The

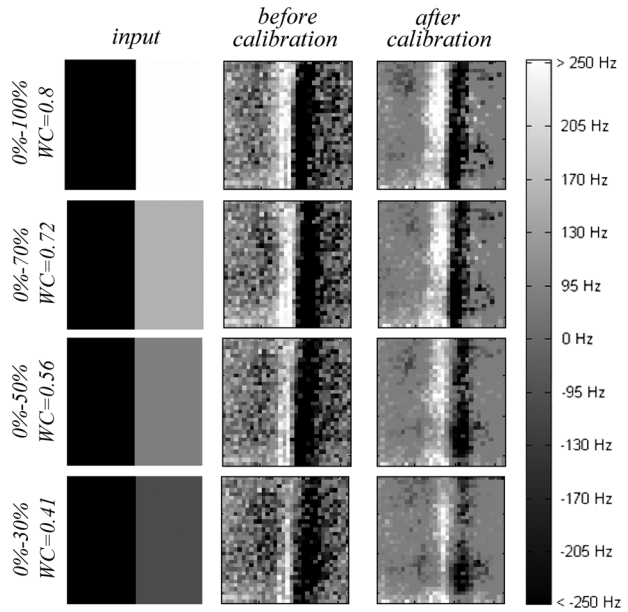

Fig. 11. Retina response to a luminance step of changing Weber Contrast. The left column is the input stimulus. The center column is the output response before calibration, and the right column is the output response after calibration.

TABLE III
RELATIONSHIP BETWEEN LUMINANCE STEPS AND WEBER CONTRAST

luminance step	100% to 0%	70% to 0%	50% to 0%	30% to 0%	10% to 0%	0% to 0%
I_{light}/I_{dark}	9	6	3.6	2.4	1.5	1.0
Weber Contrast (WC)	0.80	0.72	0.56	0.41	0.20	0

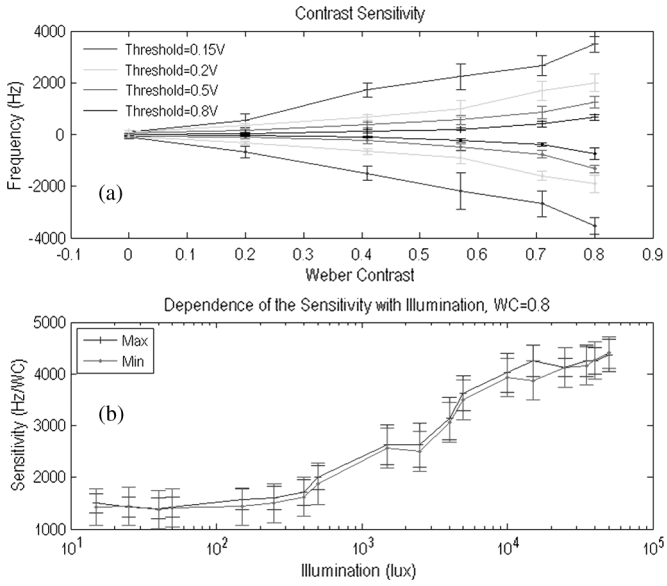

Fig. 12. Contrast sensitivity measurements. A stimulus step (as in Fig. 11) was applied, and max and min frequencies were recorded. (a) Top panel shows max and min frequencies for different stimulus step contrasts and different threshold values. (b) Bottom panel shows how the maximum and minimum frequencies depends on illumination ($WC = 0.8$).

measured maximum contrast sensitivity was 4400 Hz/WC (Hz per Weber Contrast) for $V_{\text{high}} - V_{\text{ref}} = V_{\text{ref}} - V_{\text{low}} = 0.15$ V. Error bars indicate interpixel variability.

To show the sensitivity dependence with illumination, the maximum output frequency for a Weber Contrast of $WC = 0.8$ was measured (for both signs of contrast) with different illumination levels. As shown in Fig. 12(b), sensitivity degrades slightly when illumination decreases. Sensitivity remains almost constant over the first two decades and approximately doubles over the second two decades.

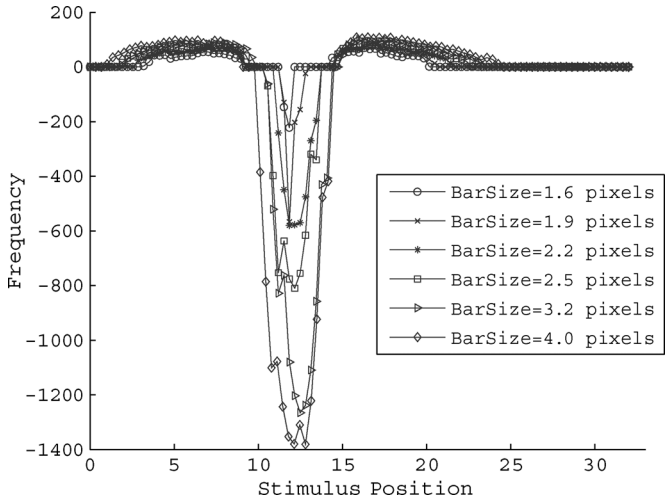

Fig. 13. Typical pixel's output when the retina is stimulated with a 100% contrast bar of different widths.

E. Contrast Thresholding

In Fig. 13, the typical pixel output, when the visual field is swept with a gray level bar stimulus of $WC = 0.8$, is shown. The x-axis indicates bar position in row number units. The pixel output spike frequency reaches the maximum value when the stimulus is at the pixel's row. This value depends on the width of the sweeping bar. Several outputs using different bar widths have been plotted for the same pixel. The bar width is expressed in projected pixel units. The maximum frequency is proportional to the stimulus width. In both cases, the following voltages were used: $V_{\text{high}} = 2.9$ V, $V_{\text{low}} = 1.4$ V, and $V_{\text{ref}} = 1.65$ V. With these settings, $V_{\text{high}} - V_{\text{ref}} > V_{\text{ref}} - V_{\text{low}}$; thus, negative events were enhanced.

It is also possible to fully inhibit positive or negative events by setting either I_{high} or I_{low} [see Fig. 5(e)] to sufficiently large values. Asymmetrical thresholds ($I_{\text{low}} \neq I_{\text{high}}$) can also be used. Therefore, positive and negative events can be inhibited independently. In Fig. 14, the effect of thresholding is shown. First, the visual field was swept with a 100% contrast bar for different thresholds. Fig. 14(a) shows the output frequency for pixel (17, 11) when setting symmetric thresholds. Fig. 14(b) shows the same pixel results but when setting only threshold values to inhibit positive events. The negative output frequency remains constant.

The main advantage of thresholding is to remove the residual mismatch after calibration. Pixels usually spike with a low residual output frequency after calibration. Positive and negative thresholds can be set to remove these undesirable outputs after calibration. Fig. 14(c)–(e) shows some snapshots captured with the contrast retina. Central gray color indicates zero output (no contrast). Positive events range from this gray to black, and negative events range from this gray to white. The three snapshots were taken for different values of the positive

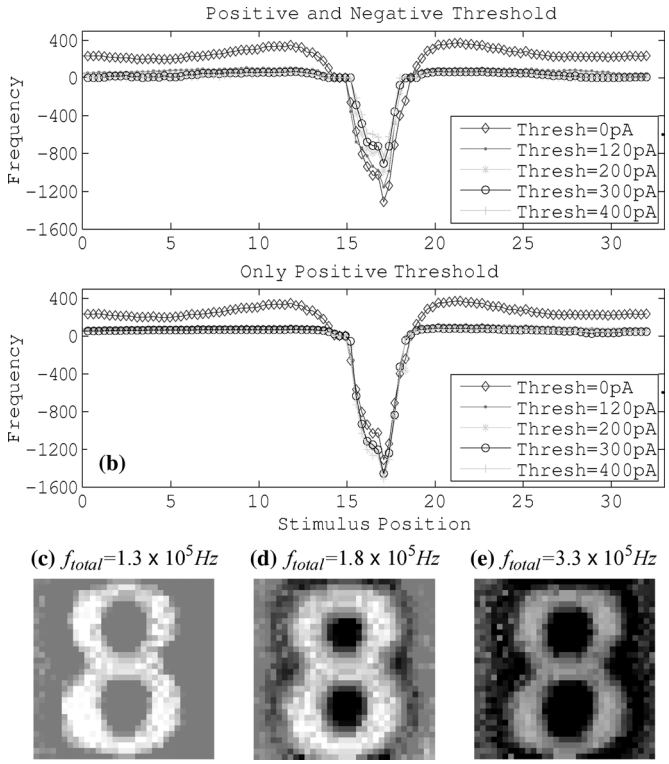

Fig. 14. Effect of thresholding. (a) Bar is swept for different symmetric thresholds. (b) No threshold for negative events, and positive event thresholds are changed. (c) Events captured for calibrated retina when all positive events are inhibited by setting a high positive threshold. (d) Events captured for calibrated retina with symmetric threshold. (e) Events captured for uncalibrated retina.

and negative thresholds. For the three cases, $I_u = 150$ pA. In Fig. 14(c), a positive threshold current of 1 nA was set to inhibit positive events completely after calibration. I_{low} was 150 pA. In Fig. 14(d), a symmetric threshold of 80 pA was set after calibration. In Fig. 14(e), the retina output without neither calibration nor thresholding is shown. Above each snapshot, the sum of all pixels' frequencies f_{total} is indicated. We can see, by comparing (d) and (e), that calibration reduces event flow (communication bandwidth) while enhancing contrast gain.

F. Latency Characterization

To characterize the retina latency, we proceeded as follows. We stimulated a LED with a step signal to turn it ON, focused it over a central region of the sensor array, and recorded the time delay between the step signal and the first event *Rqst* coming out of the chip from that region. The measurements were repeated by inserting different neutral density filters to attenuate light intensity from about 50 klux down to 2 lux. The resulting latencies are shown in Fig. 15. The measurement was repeated by focusing the LED over different regions of the pixel array. The bars in Fig. 15 show the spread obtained when changing this region. As can be seen, latency changes from about 10 ms down to about 0.1 ms when illumination varies over almost five decades. This means that latency is dominated by the photo-sensing circuits. However, latency does not scale proportionally to light, and consequently, this retina does not suffer from the severe Light-to-Time restriction listed in Table I.

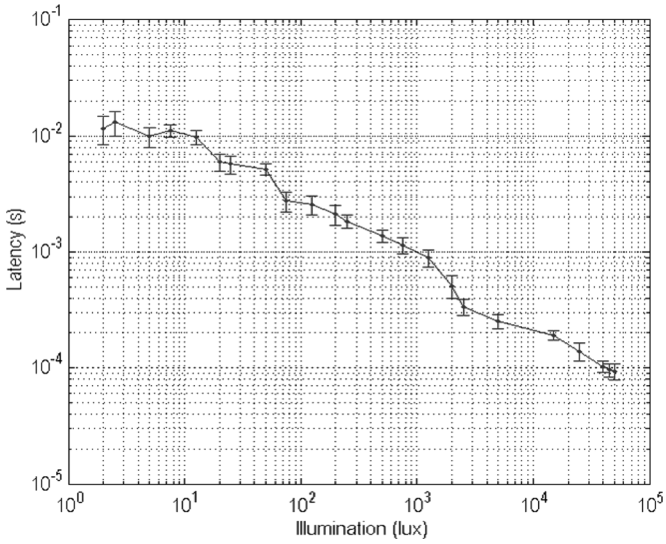

Fig. 15. Latency measurements under changing illumination conditions.

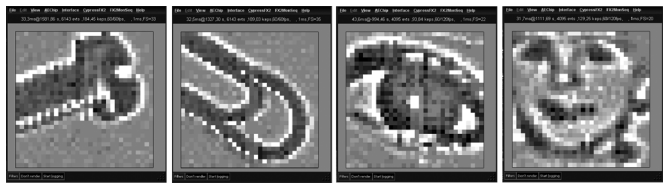

Fig. 16. Natural elements. (From left to right) Screw, paper clip, eye, and child face.

G. Natural Scenes

Although the retina resolution is rather low (32 × 32 pixels) for observing natural scenes, Fig. 16 shows some captured images when observing natural elements, which give a first-order feeling of how an up-scaled retina version would respond under a natural scene.

H. TFS Output Mode

As mentioned in Section V-B, the integrate-and-fire circuit of the retina pixel can be configured to operate in the TFS mode. In this mode, the refractory period of the retina has to be set to its largest possible value (by connecting voltage V_{rfr} to V_{dd}) to guarantee that each pixel will fire at the most one single event. Then, a periodic reset pulse has to be provided for global signal $\overline{TFS}$. This can be done in several ways. One trivial option is to reset at a fixed preset frequency. However, another more efficient option is by counting the output events. Since output events are coming out in decreasing order of pixel contrast, high-contrast pixels (either positive or negative) come out first. These are the pixels carrying more relevant information, for example, for a recognition application. Consequently, one could add a simple counter at the *Rqst* line and have it generating a reset pulse for $\overline{TFS}$ after each M events. This way, a dynamic "frame time" T_{frame} would be produced which self-adjusts to the contrast level of the scene, independent of ambient light. High-contrast scenes would self-tune to faster frames, while low-contrast scenes would self-tune to slower frames for the same amount of contrast information. Other more sophisticated options could use a postprocessing-event-based system for performing a given recognition and provide the reset pulse once a recognition has been achieved, or reset after a preset time if no recognition was

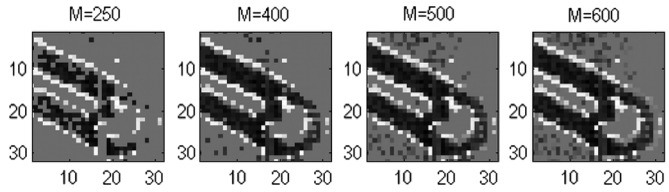

Fig. 17. Paper clip snapshots in TFS mode for different numbers of captured events M.

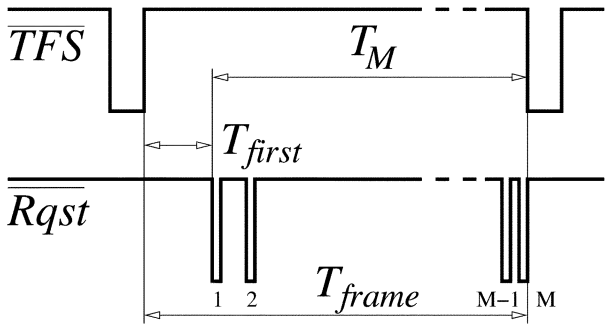

Fig. 18. Time line of the global reset and the request signal.

possible. In what follows, we count a fixed number of events M. Fig. 17 shows the effect of changing M when observing the paper clip of Fig. 16. Note that setting M to low values also removes background noise.

The TFS output mode is also insensitive to illumination (in the first order), since it operates directly on $I_{\rm cont}$ within the integrate-and-fire circuit [see Fig. 5(c) and (d)]. To show this, several snapshots of the paper clip of Fig. 17 were taken under different illumination conditions. As shown in Fig. 18, $T_{\rm frame}$ is the sum of $T_{\rm first}$ (the time the retina needs to generate the first spike after the reset) and T_M (the time between the first and Mth spike). Fig. 19 shows the value of $T_{\rm frame}$ for different values of M and illumination levels. $T_{\rm frame}$ is almost independent on illumination and is approximately constant for a given M. Fig. 19 also shows the value of $T_{\rm first}$ versus illumination. In principle, $T_{\rm first}$ should not depend on ambient light because this reset is performed within the integrate-and-fire circuit [see Fig. 5(c)] and not the photo-sensing circuit [Fig. 5(b)]. However, Fig. 19 shows a slow-down process when decreasing ambient light (between 5 klux and 200 lux, approximately). This is probably due to switching crosstalk between the integrate-and-fire and photo-sensing circuits, which introduces a switching transient in the latter that cannot be prevented when the photocurrents are too small. Such problem can be attenuated in future designs by improving decoupling between the two stages, for example, through cascoding techniques.

I. Power Consumption

Chip power consumption has been characterized. The supply voltage is 3.3 V. In principle, it would depend on both static bias conditions and output event rate. However, in practice, it is dominated by the latter because of the high consumption of digital pads communicating output events. Static power dissipation is negligible, since pixel current biases are set to relatively low values. Typical bias settings are $I_u = 150$ pA, $I_{\rm low} = 50$ pA,

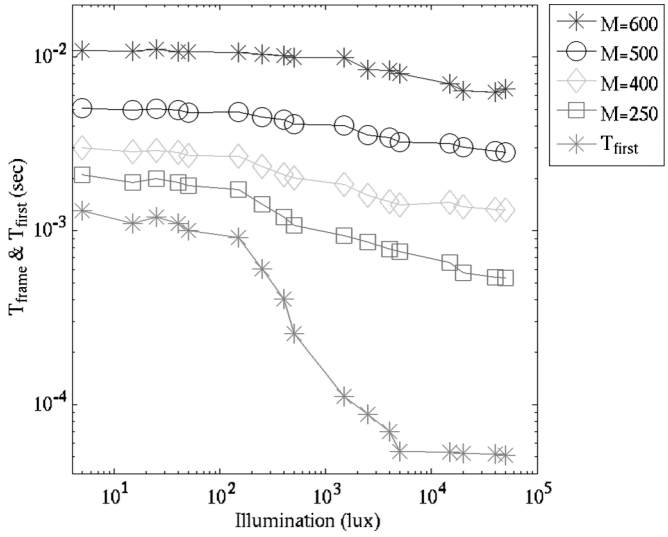

Fig. 19. Effect of illumination on $T_{\rm frame}$ and $T_{\rm first}$.

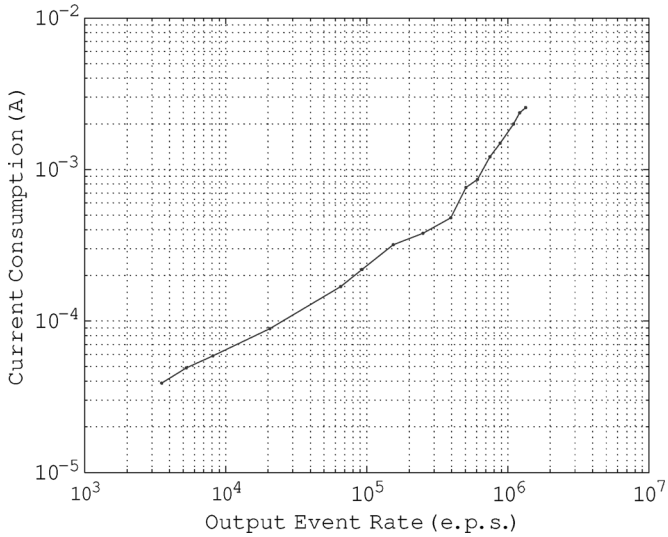

Fig. 20. Chip total current consumption as a function of total output event rate.

and $I_{\rm high} = 50$ pA. This results in a pixel static current consumption of 15 nA. At very low output event rate (1 keps), we measured a chip current consumption of 40 μA (130 μW). Fig. 20 shows the measured current consumption of the chip as a function of output event rate. As can be seen, for normal operation regimes (between 100 keps and 1 Meps), current consumption varies between 200 μA and 2 mA (660 μW–6.6 mW).

Pixel output frequency (or TFS timing) range is directly controlled by bias current I_u (see Fig. 5). Therefore, I_u controls also the overall power consumption and the speed–power tradeoff.

VII. Conclusion

A new AER signed-spatial-contrast retina has been presented. It uses an improved and calibrated version of Boahen's contrast circuit. The design avoids the problem of AER communication bandwidth consumption that is present in prior designs. Furthermore, it also includes a thresholding mechanism, so that only pixels sensing spatial contrast above a given threshold generate events. A calibration scheme is included to partially compensate for pixel mismatch. An optional TFS coding scheme is also

available. Extensive experimental results from a test prototype of 32 × 32 pixels, fabricated in a 0.35-μm CMOS technology, are provided.

An interesting advantage of this contrast retina is its fast time response, as well as low communication throughput, compared to commercial video cameras rendering full frames every 30–40 ms. Information throughput is reduced because only relevant contrast information is provided. Regarding speed response, for example, when operating in a rate-coded mode, since active pixels fire at frequencies in the range of 1–5 kHz, they would all update its state within fractions of 1 ms, independent of ambient light. In TFS mode, the first front of relevant events ($M = 250$ in Fig. 19) is available in less than 1 ms. If the stimulus changes, the retina latency depends on lighting conditions, ranging from about 100 μs at sunlight (50 klux) to 10 ms at moonlight (2 lux), with 1 ms for indoor ambient light (1 klux).

Consequently, the complexity of developing spike-based AER spatial-contrast retinae, as opposed to conventional frame-scanned video cameras, is justified by its higher speed response for a very wide range of illumination conditions, while maintaining the information throughput low and ambient light independent. Although information throughput is low, relevant (contrast) information is preserved, which results in significant processing performance improvement for subsequent stages.

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REFERENCES

[1] M. Sivilotti, "Wiring considerations in analog VLSI systems with application to field-programmable networks," Ph.D. dissertation, California Inst. Technol., Pasadena, CA, 1991.

[2] M. Mahowald, "VLSI analogs of neural visual processing: A synthesis of form and function," Ph.D. dissertation, California Inst. Technol., Pasadena, CA, 1992.

[3] E. Culurciello, R. Etienne-Cummings, and K. A. Boahen, "A biomorphic digital image sensor," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 281–294, Feb. 2003.

[4] P. F. Ruedi, P. Heim, F. Kaess, E. Grenet, F. Heitger, P.-Y. Burgi, S. Gyger, and P. Nussbaum, "A 128 × 128, pixel 120-dB dynamic-range vision-sensor chip for image contrast and orientation extraction," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2325–2333, Dec. 2003.

[5] M. Barbaro, P. Y. Burgi, A. Mortara, P. Nussbaum, and F. Heitger, "A 100 × 100 pixel silicon retina for gradient extraction with steering filter capabilities and temporal output coding," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 160–172, Feb. 2002.

[6] S. Chen and A. Bermak, "Arbitrated time-to-first spike CMOS image sensor with on-chip histogram equalization," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 3, pp. 346–357, Mar. 2007.

[7] X. G. Qi and J. Harris, "A time-to-first-spike CMOS imager," in *Proc. IEEE ISCAS*, Vancouver, AB, Canada, 2004, pp. 824–827.

[8] M. Azadmehr, J. Abrahamsen, and P. Häfliger, "A foveated AER imager chip," in *Proc. IEEE ISCAS*, Kobe, Japan, 2005, pp. 2751–2754.

[9] R. J. Vogelstein, U. Mallik, E. Culurciello, R. Etienne-Cummings, and G. Cauwenberghs, "Spatial acuity modulation of an address-event imager," in *Proc. 11th IEEE ICECS*, Dec. 2004, pp. 207–210.

[10] J. Kramer, "An integrated optical transient sensor," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 9, pp. 612–628, Sep. 2002.

[11] P. Lichtsteiner, C. Posch, and T. Delbrück, "A 128 × 128 120 dB 15 μs latency asynchronous temporal contrast vision sensor," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 566–576, Feb. 2008.

[12] M. Arias-Estrada, D. Poussart, and M. Tremblay, "Motion vision sensor architecture with asynchronous self-signaling pixels," in *Proc. 7th Int. Workshop CAMP*, 1997, pp. 75–83.

[13] C. M. Higgins and S. A. Shams, "A biologically inspired modular VLSI system for visual measurement of self-motion," *IEEE Sensors J.*, vol. 2, no. 6, pp. 508–528, Dec. 2002.

[14] E. Özalevli and C. M. Higgins, "Reconfigurable biologically inspired visual motion system using modular neuromorphic VLSI chips," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 1, pp. 79–92, Jan. 2005.

[15] G. Indiveri, A. M. Whatley, and J. Kramer, "A reconfigurable neuromorphic VLSI multi-chip system applied to visual motion computation," in *Proc. Int. Conf. Microelectron. Neural, Fuzzy Bio-Inspired Syst. Microneuro*, Granada, Spain, 1999, pp. 37–44.

[16] K. Boahen, "Retinomorphic chips that see quadruple images," in *Proc. Int. Conf. Microelectron. Neural, Fuzzy Bio-Inspired Syst. Microneuro*, Granada, Spain, 1999, pp. 12–20.

[17] K. A. Zaghloul and K. Boahen, "Optic nerve signals in a neuromorphic chip: Parts 1," *IEEE Trans. Biomed Eng.*, vol. 51, no. 4, pp. 657–666, Apr. 2004.

[18] K. A. Zaghloul and K. Boahen, "Optic nerve signals in a neuromorphic chip: Part 2," *IEEE Trans. Biomed Eng.*, vol. 51, no. 4, pp. 667–675, Apr. 2004.

[19] S. Thorpe, D. Fize, and C. Marlot, "Speed of processing in the human visual system," *Nature*, vol. 381, no. 6582, pp. 520–522, Jun. 1996.

[20] S. Thorpe, R. Guyonneau, N. Guilbaud, J.-M. Allegraud, and R. VanRullen, "SpikeNet: Real-time visual processing with one spike per neuron," *Neurocomputing*, vol. 58–60, pp. 857–864, Jun. 2004.

[21] K. Boahen and A. Andreou, "A contrast-sensitive retina with reciprocal synapses," in *Advances in Neural Information Processing*, J. E. Moody, Ed. San Mateo, CA: Morgan Kaufmann, 1992, pp. 764–772.

[22] J. Costas-Santos, T. Serrano-Gotarredona, R. Serrano-Gotarredona, and B. Linares-Barranco, "A spatial contrast retina with on-chip calibration for neuromorphic spike-based AER vision systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 7, pp. 1444–1458, Jul. 2007.

[23] T. Serrano-Gotarredona and B. Linares-Barranco, "CMOS mismatch model valid from weak to strong inversion," in *Proc. ESSCIRC*, Sep. 2003, pp. 627–630.

[24] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, Aug. 2003.

[25] J. A. Leñero-Bardallo, T. Serrano-Gotarredona, and B. Linares-Barranco, "A mismatch calibrated bipolar spatial contrast AER retina with adjustable contrast threshold," in *Proc. IEEE ISCAS*, May 2009, pp. 1493–1496.

[26] A. G. Andreou and K. Boahen, "Translinear circuits in subthreshold CMOS," *Analog Integr. Circuits Signal Process.*, vol. 9, no. 2, pp. 141–166, Apr. 1996.

[27] T. Poggio, V. Torre, and C. Koch, "Computational vision and regularization theory," *Nature*, vol. 317, no. 26, pp. 314–319, Sep. 1985.

[28] F. Gómez-Rodríguez, R. Paz-Vicente, A. Linares-Barranco, M. Rivas, L. Miro, S. Vicente, G. Jiménez, and A. Civit, "AER tools for communications and debugging," in *Proc. IEEE ISCAS*, Kos, Greece, May 2006, pp. 3253–3256.

[29] J. A. Leñero-Bardallo, T. Serrano-Gotarredona, and B. Linares-Barranco, "A calibration technique for very low current and compact tunable neuromorphic cells. Application to 5-bit 20 nA DACs," *IEEE Trans. Circuits Syst. II, Exp. Brief*, vol. 55, no. 6, pp. 522–526, Jun. 2008.

[30] K. Boahen, "Point-to-point connectivity between neuromorphic chips using address events," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 5, pp. 416–434, May 2000.

[31] R. Serrano-Gotarredona, T. Serrano-Gotarredona, A. Acosta-Jiménez, and B. Linares-Barranco, "A neuromorphic cortical layer microchip for spike based event processing vision systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 12, pp. 2548–2566, Dec. 2006.

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